MOD54415 Platform Reference

Revision History

Rev 1.0	May 12, 2012. Initial release
Rev 1.1	August 8, 2012. Changed parallel flash memory map to: 0xC1FFFFFF to reflect 32MB of memory (was 16MB).
Rev 1.2	October 11, 2012. Corrected memory map range for unused area to end at 0x3FFFFFFF.

Introduction

This document provides the memory map and locations of reference materials for those who wish to add additional hardware to their NetBurner device. Hardware dimensions, connectors and pinouts are described in the datasheet for your NetBurner device at www.netburner.com.

MCF54415 Processor Information

The Freescale reference manual and datasheet provide in-depth information on the processor and is located in the \nburn\docs\Freescale directory of your NetBurner installation.

Development Board Schematic

The MOD-DEV-70CR development board schematic is located in the \nburn\docs\platform directory. This schematic can be used for design ideas in your own hardware implementation for power, RS-232, RS-485, and SD Flash card implementation.

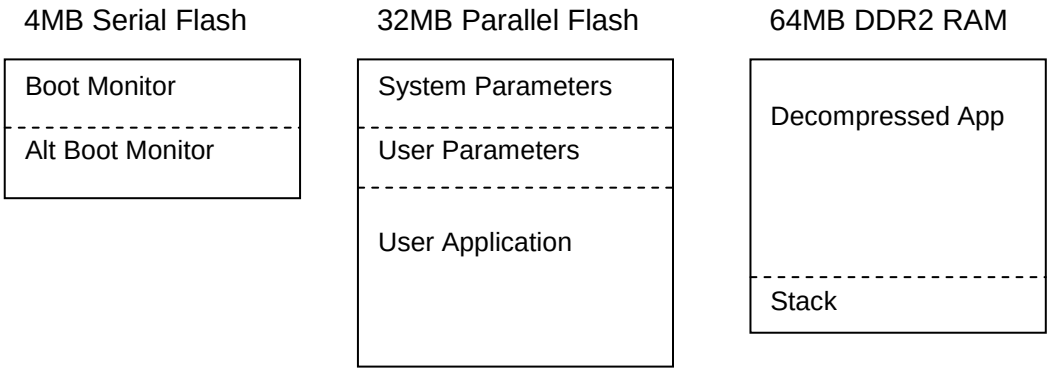
Memory Map

The MOD54415 provides 16 address lines (A0-A15) and a 16-bit data bus (D16-D31) running in mode 2. An address bus latch is included on the MOD54415 so you do not need to add an external latch. If you are adding peripherals to your NetBurner device address/data bus, you can choose unused memory locates from the table below. Once a range has been selected, you will need to configure the appropriate chip select address and option registers in the MCF54515 processor. Please refer to the chip select sections of the Freescale MCF54415 processor manual for details on the register configuration. Unlike many ColdFire processors you are not free to use any unused address for chip selects.The range is restricted. In this table we have used “undefined” for restricted ranges and “unused” for ranges that are valid for additional chip selects. Please see the MCF54418RM Section 20.3.1 and the Note above Figure 20-1 for additional details

Memory Region	Address Range	Description
Undefined	0x00000000 to 0x01FFFFFF	Undefined area to catch null pointers
Unused	0x02000000 to 0x3FFFFFFF	Available to applications
DDR2 RAM	0x40000000 to 0x43FFFFFF	64MB of DDR2 RAM
VBR	0x40000000 to 0x400003FF	1kB processor vector base register
RAMBAR	0x80000000 to 0x8000FFFF	64kB Processor internal SRAM
Parallel Flash	0xC0000000 to 0xC1FFFFFF	32MB parallel flash memory
System Config Rec	0xC0000000 to 0xC001FFFF	128kB system configuration storage
User Params	0xC0020000 to 0xC003FFFF	128kB user parameter storage
Application Code	0xC0040000 to 0xC1FFFFFF	Compressed application code
Unused	0xC2000000 to 0xDFFFFFFF	Available to applications
IPSBAR	0xE0000000 to 0xFFFFFFFF	Processor internal device registers - accessible using the SIM structure defined in sim5441x.h

Boot Monitor and Serial Memory

The MOD54415 uses a 4MB serial flash chip that provides a normal boot monitor and alternate boot monitor images. Only the parallel flash and DDR2 RAM appear in the MOD54415 memory map as described in the previous section. Using a serial flash for the boot monitor enables an easy recovery in the event an application corrupts the parallel flash.



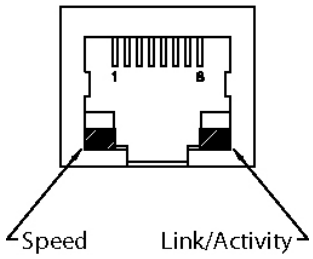
The Boot Monitor is executed first and provides a minimal boot implementation with only serial communication. The Boot Monitor will first attempt to run the User Application image in parallel flash. If the User Application is corrupted or does not exist, it will attempt to run the Alternate Boot Monitor. If the Alternate Boot Monitor cannot be run, the system will remain in the Boot Monitor and serial communication must be used to communication with the module.

The Alternate Boot Monitor extends the functionality of the Boot Monitor to include network communication so a bad User Application recovery can be done through the network rather than serial.

RJ-45 Connector

LEDs

LED 1: Ethernet speed: 10 MB (off) or 100 MB (on)
LED 2: Link/Activity



Pinout Information

Pin	Signal	Pin	Signal
1	TX+	5	----
2	TX-	6	RX-
3	RX+	7	----
4	----	8	----